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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,823	08/24/2007	Philippe Le Roy	PF030183	4918

24498 7590 06/23/2010

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EXAMINER	
RAINEY, ROBERT R	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
06/23/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/583,823	LE ROY ET AL.	
	Examiner	Art Unit	
	ROBERT R. RAINEY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/21/2006* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20060621*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-3 and 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0052614 to *Howard* ("*Howard*") in view of U.S. Patent No. 6,677,937 to *Takahashi et al.* ("*Takahashi*").

This rejection is made for lack of an inventive step since the invention may be generated by

Use of a Known Technique To Improve Similar Devices (Methods, or Products) in the Same Way

As to **claim 1**, *Howard* discloses a method and system for stabilizing thin film transistors in AMOLED displays, that is a base device, and in particular:

1. Image display screen suitable for displaying image frames, comprising:

light emitters distributed as rows of emitters and columns of emitters to form an array of emitters, the emitters of the array being able to be supplied with a current during a screen display mode (see for example Fig. 1);

an emitter addressing circuit, associated with each emitter of the array, the said circuit comprising:

a current modulator able to supply current to the said emitter, during the said display mode, the said modulator comprising a gate electrode and two current flow electrodes (see for example Fig. 2 item Q1),

a charge capacitance able to store, at each image frame, an addressing voltage representative of an image datum during the said display mode, the said voltage being applied to the gate electrode of the current modulator (see for example Fig. 2 item C1);

a control system able to apply a bias voltage to the gate electrode of the current modulator, during a ~~screen standby mode~~ non-display time, the said bias voltage having a bias inverse to the bias of the addressing voltage applied to the said charge capacitance during the screen display mode (see for example ABSTRACT and Fig. 2),

wherein the duration of application of the bias voltage having a bias inverse to the bias of the addressing voltage is greater than the duration of an image frame (this is reasonably suggested since the inverse bias is applied at least once per frame the total application time will continue to add up for the life of the display).

Howard further discloses or reasonably suggests that the inverse voltage may be applied more frequently for shorter periods or less frequently for longer periods (see for example Fig. 4 and 5; the use of shorter versus longer time periods is reasonably suggested by the fact that more non-display time is available between frames than between rows) and the use of different inverse

voltage bias levels to compensate for different levels of forward voltage bias induced drift (see for example [0030] especially "The reverse voltage in the embodiment of FIG. 3A is determined either by reference to the data current signal or by reference to an average data signal level".; should applicant feel that further reasonable suggestion is required to identify the use of shorter versus longer periods, examiner notes that increasing inverse bias time was a known alternative to increasing inverse bias voltage)

Howard does not expressly disclose that the inverse bias is applied during a screen standby mode.

Takahashi discloses a driving method for display and a liquid crystal display using such a method and in particular:

A comparable device (method, or product), that is not the same as the base device. The device is comparable for several reasons: first because it is a display device; second because elements of its pixels suffer from the same problem, which is bias-voltage induced drift (see for example Fig. 7 item 72 and 2:21-39 especially "The active-matrix type liquid crystal display 51 using two-terminal elements 72 has a problem in which a sticking phenomenon occurs due to variations in the voltage-current characteristics of the two-terminal elements 72." or Fig. 7 item 71 the liquid crystal element), and it attempts to solve the problem in the same way, which is by applying an inverse voltage on a periodic basis during a display time (see for example Fig. 9 PRIOR ART).

Improvement of the comparable device in the same way as the claimed invention and in particular:

a control system able to apply a bias voltage to the drift sensitive element (see for example Fig. 7 items 71 or items 72), during a screen standby mode (see for example Fig. 1 especially "OUTPUT OF NON-LIT-UP DISPLAY DATA" or ABSTRACT especially "The display elements are maintained in the non-lit-up display state over the entire surface of the display up to completion of a period corresponding to a predetermined number of frames after the frame in which the power-supply OFF signal has been detected."; note a power-supply OFF signal with respect to the display reasonably suggests a screen standby mode since it was known to shut down the display both during a screen standby mode as well as during a complete power-off cycle), the said bias voltage having a bias inverse to the bias of the addressing voltage applied to a charge capacitance during the screen display mode (see for example 9:23-45 especially "Then, the respective pixels are switched to a lit-up state (driven state) when the accumulated charge reaches not less than a predetermined value, and also switched to a non-lit-up state (non-driven state) when the charge has been drawn to reach not more than a predetermined value.", the voltage applied in the is inverse to the one used to create the driven state since it removes the charge accumulated in the driven state.);

wherein the duration of continuous application of the bias voltage having a bias inverse to the bias of the addressing voltage is greater than the duration of

an image frame (see for example Fig. 1 especially the time period of "OUTPUT OF NON-LIT-UP DISPLAY DATA" versus the time period of each frame, which is that of the "EFFECTIVE DISPLAY PERIOD" plus the "NON-DISPLAY PERIOD").

One of ordinary skill in the art could have applied the known improvement technique of *Takahashi* in the same way to the base device (method, or product) of *Howard* and the results would have been predictable to one of ordinary skill in the art. One of ordinary skill could have applied the improvement technique because the circuitry to apply the inverse voltage was already available in the device of *Howard* and *Takahashi* taught the modifications necessary to implement a period of inverse voltage application longer than a frame time after a command for display shutdown. The results would have been predictable because the effect of inverse voltage application in the device of *Howard* was known and thus the effect on the current modulator would have been known and Takahashi taught or reasonably suggested the effects related to timing, such as a longer period of power application after a shut-down command.

As a further evidence of obviousness consider that *Takahashi* also offers a suggestion/motivation to implement the improvement, which would have been to provide advantages such as to ensure that the display reaches a blank state quickly (see for example 14:18-30 especially "since the quantity of charge of the display panel becomes uniform on all the pixels after the non-lit-up display over

the entire surface has been provided, it becomes possible to positively eliminate remaining images").

As to **claim 2**, in addition to the rejection of claim 1 over *Howard* and *Takahashi*, *Howard* further discloses

2. Display screen according to claim 1, wherein the control system comprises addressing control means able to apply on the one hand the said addressing voltage to the gate electrode of the current modulator during the screen display mode and, on the other hand, the said bias voltage during the screen standby mode (see for example Fig. 2A).

As to **claim 3**, in addition to the rejection of claim 1 over *Howard* and *Takahashi*, *Howard* and *Takahashi* does not expressly disclose:

3. Display screen according to claim 1, wherein the control system comprises means of control of scanning of the lines of the screen that are adapted for decreasing the frequency of scanning of the lines of the screen during the screen standby mode to a frequency below the frequency of scanning of the lines during the display mode.

However, reduction of scanning frequency for power saving in the case of static images was known. Since the display in this case is static, that is the data voltage does not change from frame to frame, the application of the known power saving improvement would have been obvious.

As to **claim 7**, in addition to the rejection of claim 1 over *Howard* and *Takahashi*, it was known to cut off power supply to emitters in a display, which otherwise continues to be powered, when the emitters should not display in order to prevent unwanted display or to save power. An example of this is found in some types of drive voltage programming, which cuts off power supply to the emitters during the time that the drive voltage is being programmed and thus does not represent a valid display voltage. Thus it would have been obvious to provide the device after *Howard* and *Takahashi* with additional capability to provide:

7. Display screen according to claim 1, wherein it comprises means for supplying power to the emitters and in that the control system comprises means for cutting the supply to the emitters during the screen standby mode.

3. **Claims 4-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0052614 to *Howard* ("*Howard*") in view of U.S. Patent No. 6,677,937 to *Takahashi et al.* ("*Takahashi*") and further in view of U.S. Patent No. 5,444,457 to *Hotto* ("*Hotto*").

As to **claim 4**, in addition to the rejection of claim 1 over *Howard* and *Takahashi*, *Howard* and *Takahashi* may not expressly disclose:

4. Display screen according to claim 1, wherein the control system comprises means of calculation of the sum of the said voltages applied, at each image frame, to the gate electrode of each current modulator during the screen display mode, the said means of calculation being able to determine characteristics of a bias voltage suitable for being applied to each current modulator, as a function of the said sum of the said voltages applied to this modulator, and in that the control system is able to apply, to each modulator, the said suitable bias voltage determined by the means of calculation, during the screen standby mode.

Hotto discloses a DC integrating display driver employing pixel status memories and in particular:

4. Display screen according to claim 1, wherein the control system comprises means of calculation of the sum of the said voltages applied, at each image frame, to a voltage-bias sensitive element during the screen display mode, the said means of calculation being able to determine characteristics of a bias voltage suitable for being applied to each voltage-bias sensitive element, as a function of the said sum of the said voltages applied to this voltage-bias sensitive element, and in that the control system is able to apply, to each voltage-bias sensitive element, the said suitable bias voltage determined by the means of calculation (see for example 2:1-24 especially "... the use of memory and computation means to simulate the condition of the display in real time. ...The

bias status can, therefore, remain or accumulate in one polarity for multiple display periods.").

Howard and *Takahashi* and *Hotto* are analogous art because they are from the same field of endeavor, which is display drive circuitry, and seek to solve the same problem, which is to mitigate the effect of accumulated voltage stress on voltage-stress sensitive pixel elements.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to apply the teachings of *Hotto* to the combination of *Howard* and *Takahashi* such that:

The control system comprises means of calculation of the sum of the said voltages applied, at each image frame, to the gate electrode of each current modulator during the screen display mode, the said means of calculation being able to determine characteristics of a bias voltage suitable for being applied to each current modulator, as a function of the said sum of the said voltages applied to this modulator, and in that the control system is able to apply, to each modulator, the said suitable bias voltage determined by the means of calculation, during the screen standby mode.

The suggestion/motivation would have been to provide advantages such as to decrease the frequency of reverse bias application or provide greater flexibility in element driving during display operations (see for example Hotto 7:26-48 especially "Thus, the polarity of the drive signals does not need to be reversed until one or more pixels approach MBVT.").

As to **claims 5 and 6**, in addition to the rejection of claim 4 over *Howard* and *Takahashi* and *Hotto*, the fact that increasing inverse bias time was a known alternative to increasing inverse bias voltage was covered in claim 1 and thus it would have been obvious to provide:

5. Display screen according to claim 4, wherein the characteristics of the bias voltage that are determined by the means of calculation comprise the duration of application of the bias voltage.

6. Display screen according to claim 4, wherein the characteristics of the bias voltage that are determined by the means of calculation comprise the value of the said bias voltage.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5012314 to Tobita et al. teaches TFT adjustment offline by irradiation - an extreme example of off-state processing.

US 20050007352 to Nathan et al. Fig. 5 and 6 and [0045]-[0046] teach voltage/time dependence of TFT threshold shifts.

US 7151513 to Li et al. teaches the application of inverse bias through data lines during the display time.

US 6069620 to Nakamura et al. teaches performing compensation for a period longer than a frame period after pressing power-on button. DETX(29) power-on reset period longer than 15 sec -- to put the LC material into the correct state.

US 7170094 to Yamazaki et al. teaches inverse voltage larger for longer display periods - interchangeability of longer time and larger voltage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINEY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/

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